

SINGLE CHIP RADIO IC INCLUDING SYNCHRONOUS DETECTOR

Taiwa Okanobu
Sony Corporation
Tokyo, Japan

Daisuke Yamazaki
Sony Corporation
Atsugi, Japan

Abstract

A new single chip AM/FM radio IC for short wave receiver has been developed. It includes synchronous detector, PSN, AM detector, and SSB detector. And distortion and characteristic for various interferences have been improved.

Introduction

At AM broadcast, especially the condition of short wave broadcast often becomes poor by fading or adjacent frequency signal interference. Synchronous detector will improve it. By generating carrier in receiver, over modulated distortion which is brought about by carrier suppression caused by fading can be improved, and adjacent frequency signal interference also can be reduced by the choice of the side band (USB or LSB).SSB has already been used for communication, and reduced carrier SSB

broadcasting has started its service recently, therefore many communication receiver has synchronous detector, but few consumer receiver has it.

Conventional Radio

In conventional consumer short wave radio, most of the detector circuits are envelope detector by diode and product detector (few radio has it) for SSB decoding. Due to the scale of the circuit, radio could not be small without using new IC. And local oscillator stability and IF filter selectivity should be totally improved.

Outline of the new IC

Fig. 1 shows the block diagram of FM/AM radio using this new IC. The IC include FM front end, IF pre amplifier, FM IF limiter, FM detector, meter driver, station detector, AM 2nd mixer, AM 2nd oscillator, AM IF amplifier, and AM synchronous detector, phase shifter,

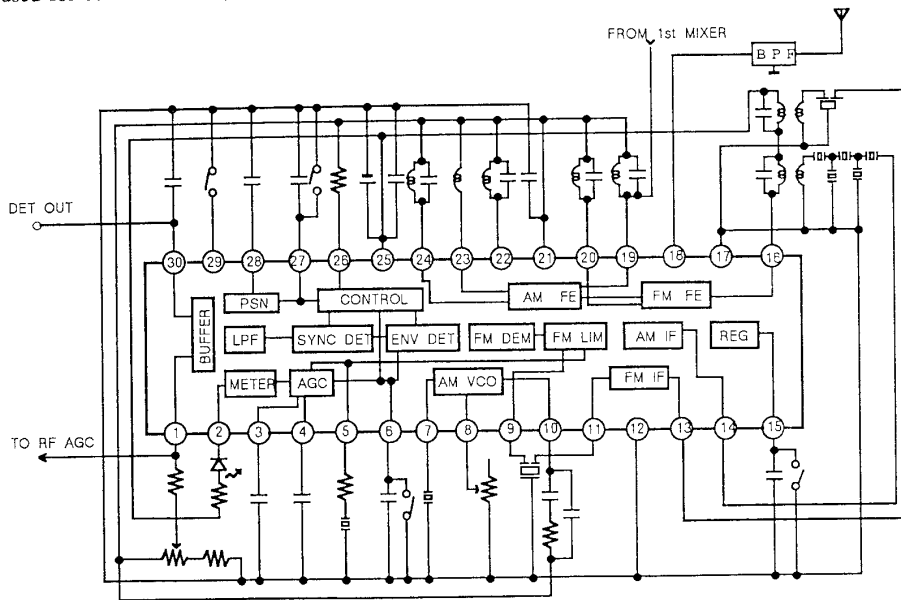


Fig.1 Block Diagram of IC

matrix, 3KHz lpf, tuning indicator driver. Double conversion is settled for HF/MW receiver and its 1st local oscillator is synthesized by PLL. FM detector is quadrature detector using ceramic phase shifter. Synchronous detector, product detector and envelope detector are available for short wave reception. USB or LSB can be selected by product detection or synchronous detection mode.

Advantage of new IC application

In comparison with conventional radio IC, the application of new IC has following advantages.

1. Advanced HF/MW/FM Radio receiver can be realized by new IC easily.
2. Short wave reception can be realized by three detector.(Synchronous detector, Product detector, Envelope detector)
3. Adjacent frequency signal interference is reduced by the selection of side band.

AM Detector Section

Fig.2 shows the block diagram of AM detector section. It consists of minimum combination of multiplier and low pass filter. In-phase synchronous detector and quadrature detector for AM synchronous and SSB detection, phase detector for PLL, envelope detector for AM envelope detection and AGC, are required for the system. Detected

signals from two synchronous detector passing PSN (Phase Shift Network : 4th order all pass network) and Matrix are separated to USB (Upper Side Band) or LSB (Lower Side Band). Built in 3KHz LPF is useful at short wave reception to avoid beat signal and stinging noise. In SSB mode, PLL loop is open ,so VCO frequency is fixed by external resistor, and detector operates as product detector.

AM IF Buffer

Fig.3 shows the PLL and synchronous detector section. The most important factor in this section is how to reduce the effect of residual phase error ' ϕ '. In the PLL loop, regenerated I/Q carrier has phase difference between input carrier (IF) due to the phase delay of limiter amplifier, and PLL locks delayed carrier $\cos(\omega t + \phi)$.

In phase detector and quadrature detector have undesired component ' ϕ ' in their output formula and effects on the side band separation. But it is impossible to make high gain limiter amplifier without phase delay, so we have compensated it by inserting AM IF buffer which has same phase delay ' ϕ ' and 0dB gain. This circuit was designed very carefully through transient analysis instead of ac analysis. Relative phase error between two amplifiers is also minimized by the matching of component characteristics on same chip.

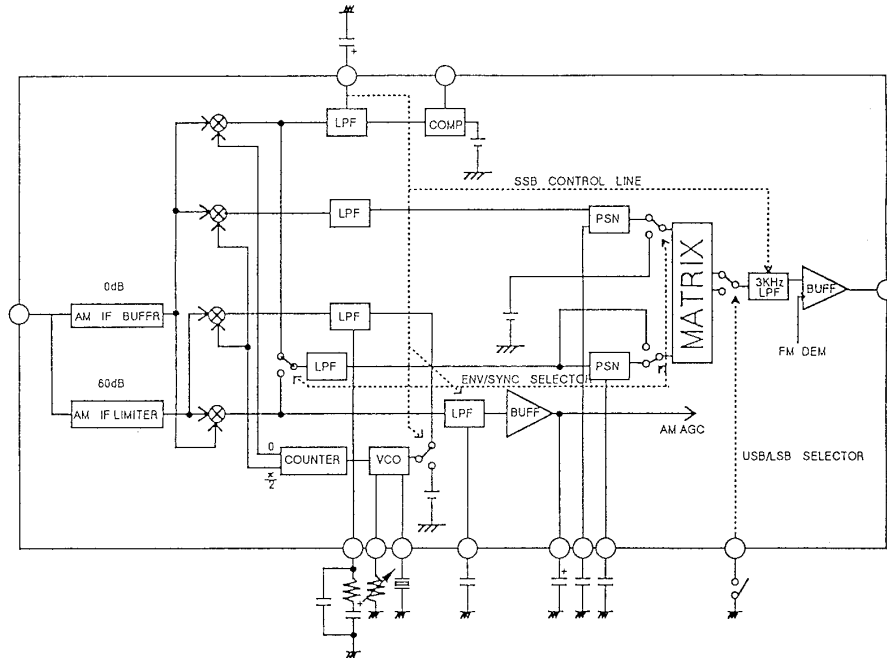


Fig.2 Block Diagram of AM Detector Section

Synchronous Detector

Synchronous detector has many advantages compared with conventional detector such as envelope detector. In envelope detector, distortion is directly effected by carrier level. Especially at short wave reception, signal would be distorted by over modulation due to the carrier suppression caused by fading. But regenerated carrier by PLL can solve this problem. Once PLL loop has locked, regenerated carrier keeps its frequency and level the signal is detected in low distortion. And another advantage is reduction of the adjacent frequency interference. Fig. 4 shows the side band spectrum interfered by undesired signal. Combination of synchronous detector, PSN, and MATRIX make it possible to separate the side band easily. Let us suppose that the desired signal V_A and undesired signal V_B come to the I/Q detector.

$$V_A = A(1+m) \sin \omega_1 t$$

$$V_B = B(1+n) \sin \omega_2 t$$

And V_I and V_Q is the regenerated carrier by PLL.

$$V_I = k \sin \omega_1 t$$

$$V_Q = k \cos \omega_1 t$$

$$(V_A + V_B) \times V_I \rightarrow 1/2 \times (1+m)A + 1/2 \times (1+n)B \cos(\omega_2 - \omega_1)t$$

$$(V_A + V_B) \times V_Q \rightarrow 1/2 \times (1+m)A - 1/2 \times (1+n)B \sin(\omega_2 - \omega_1)t$$

These out put from I/Q detector (after LPF) are converted into VD_1 and VD_2 by PSN. (phase shift network)

$$VD_1 = 1/2 \times (1+m)A + 1/2 \times (1+n)B \cos(\omega_2 - \omega_1)t$$

$$VD_2 = 1/2 \times (1+m)A - 1/2 \times (1+n)B \sin(\omega_2 - \omega_1)t$$

$$VD_1 - VD_2 = 1/2 \times (1+m)A \text{ ----- LSB}$$

$$VD_1 + VD_2 = 1/2 \times (1+m)A + (1+n)B \cos(\omega_2 - \omega_1)t$$

----- USB (by adjacent signal)

Here we could separate clean side band from the interfered signal by adjacent frequency perfectly. Fig.5 shows the I/O characteristics of synchronous detection mode.

In SSB signal reception, VCO will be fixed at proper frequency. Detection is made by the same circuit as synchronous detection. Fig.6 shows the I/O characteristics of product detection mode, and Fig.7 shows the detective signal distortion vs modulation of AM IF in envelope detection mode and SSB detection mode receiving -6dB reduced carrier SSB. At envelope detection mode harmonic distortion is serious for modulation factor.

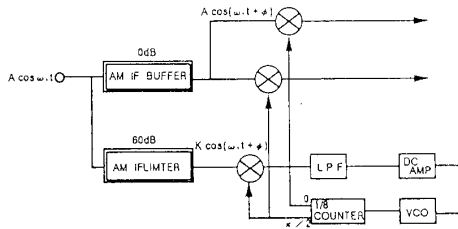


Fig.3 PLL And Synchronous Detector

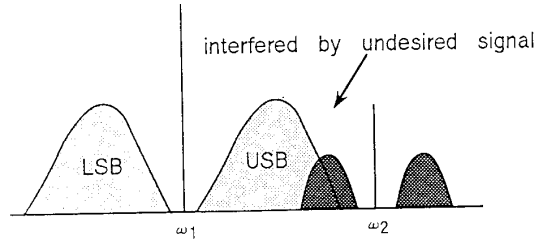


Fig.4 Side Band Spectrum

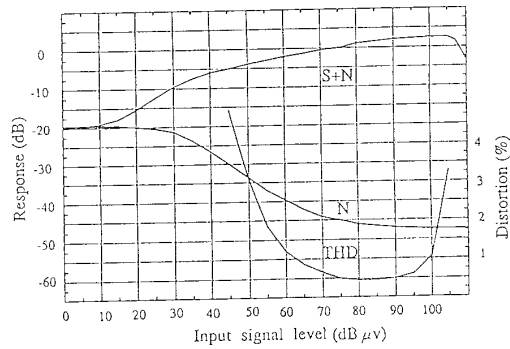


Fig.5 AM I/O Characteristics (SYNC mode)

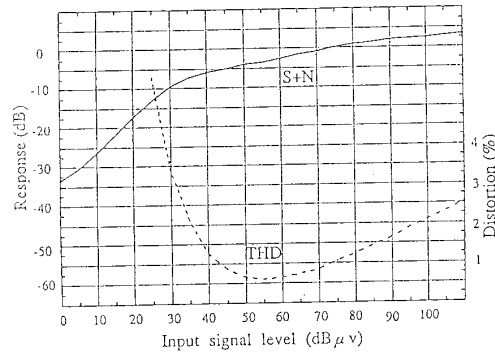


Fig.6 AM I/O Characteristics (SSB mode)

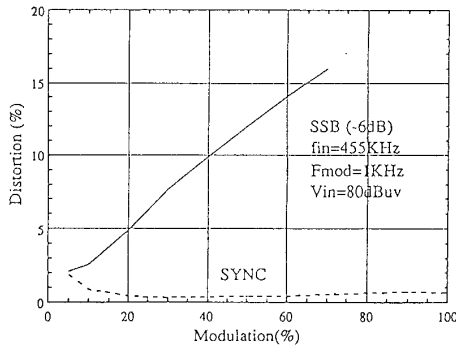


Fig.7 Distortion VS Modulation

Envelope Detector

In this IC, envelope detection is made by multiplying input signal by limited itself. And it is also used as AGC voltage after LPF in every detection mode. In SSB mode, AGC LPF is switched its response to attack faster and release slowly. Fig.8 shows I/O characteristics of envelope detection.

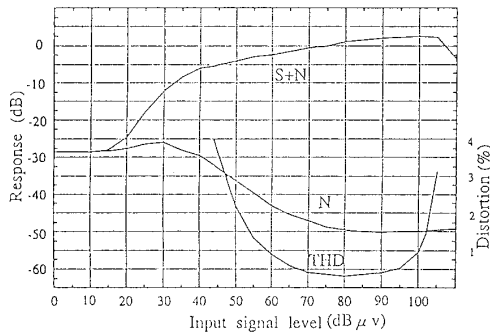


Fig.8 AM I/O Characteristics (ENV mode)

PLL

VCO operates 8 times higher than AM IF frequency, (3.64MHz or 3.60MHz) using ceramic or lithium tantalate resonator for good stability and adjustment free. VCO varies +/- 2KHz (at IF frequency) by the internal variable capacitance, VCO frequency is determined by the gain of gm amplifier. And C/N (carrier to noise ratio) is important for S/N on synchronous detection. By the calculation side band noise level needs more than 79dB (at 10Hz bandwidth) to get over 40dB signal to noise ratio ($m=0.3$). Fig.9 indicates the block diagram of PLL with loop gain controller. We had made the experiments several time for

PLL circuit with detector, and found the necessity of loop gain control. In general, PLL loop has narrower capture range than lock range, but wide capture range allows large residual phase error and miss capture for the strong undesired signal. New PLL system has wide capture range and lock range, and prevents interference from hearing by controlling loop gain. Capture range is almost the same as lock range on locking up, and then loop gain is reduced to 1/100 after lock up. As the result, selectivity to signal close to carrier frequency and a purity of regenerated carrier signal become better. Fig.10 shows the improvement on the selectivity of new PLL.

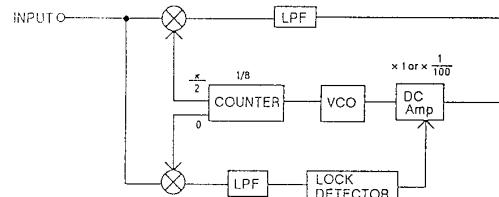


Fig.9 Loop Gain Control

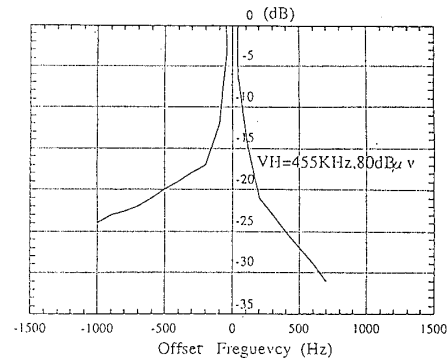


Fig.10 Selectivity of PLL

Phase Shift Network

The modified block diagram of PSN is shown in Fig.11. PSN is 4th order all pass network to match the phases of I/Q detector output, then side band separates into USB and LSB. PSN is consists of combination of OP amplifier in actual circuit, and miller capacitor is useful to build in long time constant on chip, therefore 4th order all pass network need only two external capacitance, in addition one of them

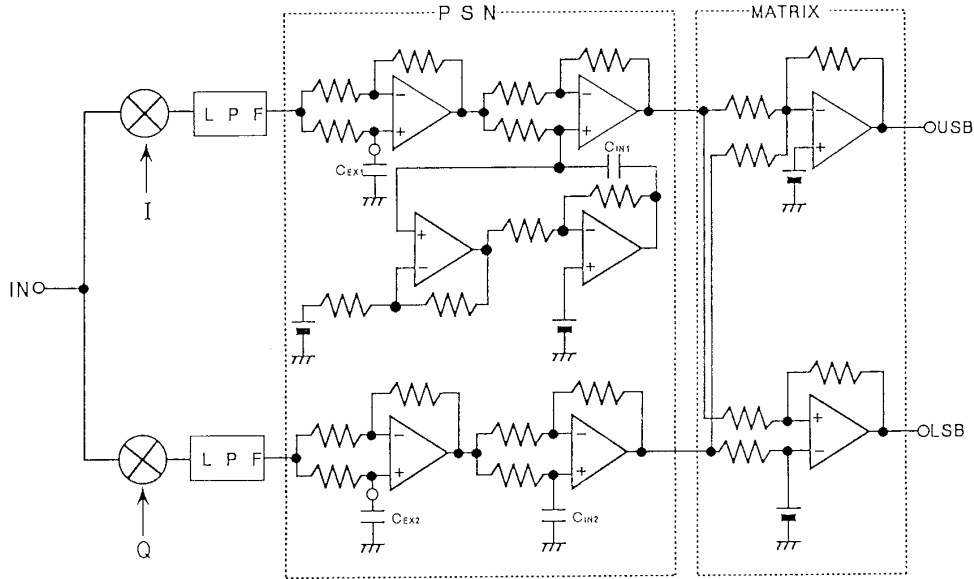


Fig.11 Modified Block Diagram of PSN

is used as a switch for mode selection (Envelope detection or Synchronous detection). Typical signal level in PSN is -40dBm, determined by the gain of miller amplifier because of its dynamic range. Side Band Suppress Ratio (SBSR) is sensitive for phase error of PSN and gain error of the detected signal level. Phase error coming from unbalance of time constant ($R \times C$) between two filters is compensated by relativity among components (resistor and capacitor) on chip. And gain error also expect them. To reach more than 30dB SBSR, it needs less than 3degree phase error or 6% gain error finally. Fig.12 indicate the frequency response of USB and LSB after 3KHz LPF at USB mode.

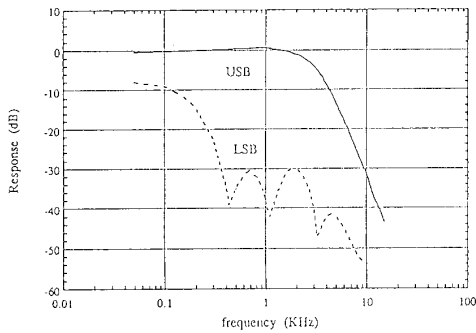


Fig.12 Frequency Response of USB/LSB

FM Section

In FM section, there are RF amplifier, Oscillator, Mixer, IF Pre-amplifier, IF limiter, Quadrature detector, tuning indicator driver, and Station detector. Ceramic phase shifter is used for Quadrature detector to realize adjustment free and good performances. RF input impedance is settled at 75ohm to get low noise figure combining with B.P.F.. Mixer (double balanced mixer) is isolated from Oscillator by oscillator buffer amplifier to avoid interference at extremely high RF input level. IF Pre-amplifier has 10dB gain to compensate for insertion loss by two IF ceramic filter. For synthesized tuning, there is a Station detector function operated by the dc voltage from S curve characteristic to tune accurately. And there is a pin for null voltage adjustment to compensate for dc offset caused by the components variation on the chip and ceramic discriminator. This is great advantage for synthesized radio manufacture. Fig.13 indicates the over all I/O characteristics in FM mode. In our application, we have got S/N of 30dB and sensitivity of $8\text{dB } \mu\text{v}$.

The Configuration of the IC

The IC is packed in the 30pin SDIP (shrink DIP) and SOP (Small Outline Package). IC chip photograph is shown in Fig.14. 1500 elements are integrated in a space $3.54\text{mm} \times 4.19\text{mm}$.

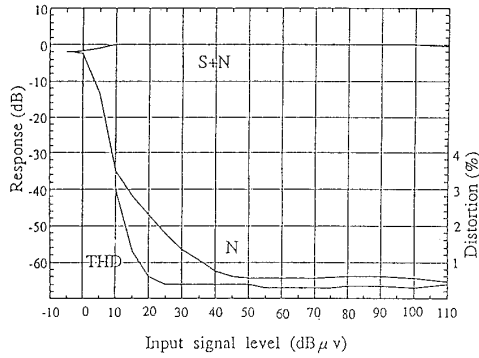


Fig.13 FM I/O Characteristics

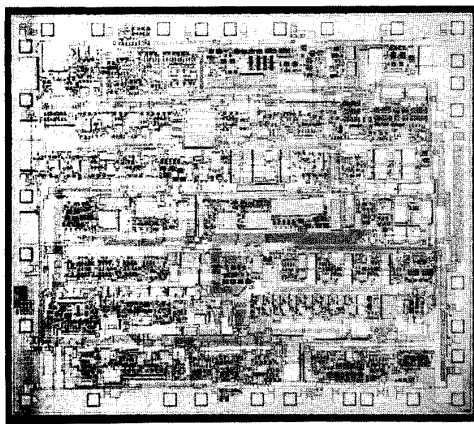


Photo 1 Photograph of the IC

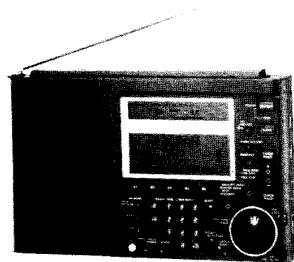


Photo 2 Photograph of the HF/MW/FM RADIO receiver applied this IC

Conclusion

A single chip radio IC including synchronous detector has been developed. The IC achieves good performance, as is shown in Table I. Also, we've managed to reduce the number of peripheral components, as well as the area and cost, and succeeded to apply this device into consumer radio receiver.

Table I Performance of the IC

Supply Voltage	2~5V
Supply Current	AM mode 14.4 mA (typ.) FM mode 10.3 mA (typ.)
FM det output level	-21.0 dBm (typ.)
FM det output distortion	0.3% (typ.)
FM IF knee level	25.5 dB μv (typ.)
AM det output level (ENV)	-21.0 dBm (typ.)
AM det output distortion	0.6% (typ.)
AM det output level (SYNC)	-21.0 dBm (typ.)
AM det output distortion	0.6% (typ.)
AM det output level (SSB)	-15.0 dBm (typ.)
AM det output distortion	0.6% (typ.)
Side Band Suppress Ratio	30dB (typ.)

odBm=0.775 Vrms

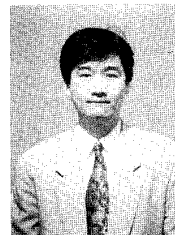
Acknowledgement

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Biographies



Taiwa Okanobu, Chief engineer of Personal Telecommunications Group, received his B.S. in Electronic Engineering from Chiba Institute of Technology, Chiba, in 1966. In 1966, he joined Sony Corporation and participated in the development of Radio and LSI for Radio and Telecommunication. He is a member of the Institute of Electronics Information and Communication Engineer of Japan.



Daisuke Yamazaki, Assistant manager of Bipolar Design Department, received his B.S. in Metallurgical Engineering from Waseda University, Tokyo, in 1982. In 1982, he joined Sony Corporation and has been engaged in the development of LSI for Radio and Analogue Audio.